

REMARKS

Applicants have amended claim 21 to correct a grammatical error and not in response to the Examiners rejection of claim 21.

The Examiner objected to claims 1, 4, 6, 7, 11, 14, 17, 27, 29.

The Examiner rejected claims 11-20 under 35 U.S.C. § 112, second paragraph, as allegedly being incomplete for failing to provide steps of the claims and that the claims are not clear as to whether they are claims for making or using.

The Examiner rejected claims 1-30 on the ground of nonstatutory obviousness-type double patenting as allegedly being unpatentable over claims 1-20 of U.S. Patent No. 7,103,832.

Applicant respectfully traverses the claim objections and § 112, and double patenting rejections with the following arguments.

Claim Objections

The Examiner objected to claims 1, 4, 6, 7, 11, 14, 17, 27, 29 stating: “As to claims 1, 7, the variables "W" and "M" are not defined in the claims. As to claim 4, it is not clear as to what is meant by "wherein B is the is the maximum" in line 1 of the claim. As to claims 6 and 7, 11, 14, 17, 27 and 29, the variables A, B, (Y-1), J, W, (A-1) are not clearly defined in the claims. Appropriate correction is required.”

Applicants have amended claims 7, 17 and 29 to remove the term (Y-1) and claims 26 and 27 to remove the term M-bits.

Applicants have amended claims 1, 4, 6, 11 and 14 to clearly define variables W, M, A, B, J, and (A-1).

(1) Applicants have amended claims 1 and 11 to indicate the packet data slice latch has W-bits and the CRC remainder latch has M-bits and Applicants have defined W and M in claims 1 and 11 as positive integers. Applicants contend that one of ordinary skill in the art would know M and W must be positive integers as there can be no fractional bits or negative bits or a zero number of bits.

(2) Claims 4 and 14 clearly define A and B, to wit :“ B is a positive integer and is the maximum number of XOR operations to be performed in a single remainder XOR subtree level of said remainder partition” and “A is a number of remainder XOR subtree levels of said remainder partition.” Applicants contend that one of ordinary skill in the art would known B must be a positive integer as there can be no fractional operations or negative operations or no operations.

(3) Claim 6 clearly defines B, to wit “the maximum number of inputs to any data XOR subtree in any data XOR subtree level of said data partition is B.” Applicants have further

defined B as a positive integer in claim 6. Applicants contend that one of ordinary skill in the art would know B must be a positive integer as there can be no fractional subtrees or negative subtrees and there cannot be a zero number of subtrees

(4) Applicants have amended claims 7 and 17 to more clearly define J.

(5) Applicants have amended claim 27 to more clearly define M.

(6) Applicants contend that claim 27 clearly defines I, A, B and (A-1), to wit:

“determining I, a largest number of bits of a subset of the M-bits of a CRC remainder”,

“determining B, a maximum number of XOR operations to be performed in a single remainder XOR subtree level of said remainder partition” and “calculating A, a number of XOR subtree levels in said remainder partition.” Further Applicants contend that one of ordinary skill in the art would read A and B as positive integers as any other reading would not make sense. There can be no partial operations, subtrees or negative operations or subtrees or a zero number of operations or subtrees. Thus, A-1 is simply a number having a value one less than A.

(7) Applicants have amended claim 29 to more clearly define J. Applicants contend that one of ordinary skill in the art would read J as a positive integer as any other reading would not make sense. There can be no negative or fractional bits or a data slice of zero bits.

Therefore Applicants respectfully request withdrawal of the Examiners objection to claims 1, 4, 6, 7, 11, 14, 17, 27 and 29.

35 U.S.C. § 112, Second Paragraph

The Examiner rejected claims 11-20 under 35 U.S.C. § 112, second paragraph, as allegedly being incomplete for failing to provide steps of the claims and that the claims are not clear as to whether they are claims for making or using.

In response, Applicants have amended the preamble of claim 11 to state the claim is to a method “for performing a cyclic redundancy check” and to included the steps of connecting the circuit elements together and performing a CRC calculation.

Double Patenting

The Examiner rejected claims 1-30 on the ground of nonstatutory obviousness-type double patenting as allegedly being unpatentable over claims 1-20 of U.S. Patent No. 7,103,832.

The Examiner stated: “claims 1, 11, 21 and 26 of the present application (No. 10/709,794) and claims 1, 9 and 17 of U.S. Patent No. 7,103,832 are functionally equivalent,” and “It is obvious that both applications claim essentially the same limitations: a W-bit packet data slice latch; a remainder latch; a remainder XOR subtree; a combinational logic XOR tree; and an M-bit current CRC.”

Applicants point out that “functionally equivalent” means the all aspects of the claims being compared must be equivalent not the function that the claims perform. For example a thin film resistor and wire wound resistor are functionally equivalent in providing resistance in a circuit but are patentably distinct from each other.

The Examiner further stated “As per claims 1, 9 and 17 (7,103,832) and claims 1, 11, 21 and 26 (10/709,794), U. S. Patent serial No. 7,103,832 claims A cyclic redundancy check circuit, comprising: a W-bit packet data slice latch having outputs; a multiple level XOR subtree...; a remainder XOR subtree having inputs and outputs; a combinational XOR subtree...; a combinational XOR tree...; and an M_bit current CRC result latch....” and application with serial No. 10/709,794 claims. A circuit, comprising: multiple W-bit packet data slice latches each having inputs and outputs...; a data partition comprising multiple data XOR subtree levels...; a remainder partition comprising multiple remainder XOR subtree levels and having remainder latches between said remainder XOR subtree levels...; a combinational XOR tree...; and an M-bit current cyclic redundancy” check (CRC) remainder latch having inputs and outputs.... It is

obvious that both applications claim essentially the same limitations: a W-bit packet data slice latch; a remainder XOR subtree; a combinatorial XOR tree; and an M-bit current CRC).”

Applicants assume the Examiner is comparing Applicants claims 1 to reference claim 1, Applicants claim 11 to reference claim 9 and Applicants claims 21 and 26 to reference claim 17.

Applicants point out the Examiner has picked a small number of elements from Applicants claims and the reference claims to compare and base his case of nonstatutory obviousness-type double patenting on and that even that comparison is flawed as explained *infra*. Further, the Examiner has failed to address the connections between elements in Applicants claims and the reference claims. Still further, the Examiner has failed to cite any specific comparisons between Applicants claims 2 through 10, 12 through 20, 22 through 25 and 27 through 30 and any claims in the reference.

Specifically as to Applicants claims 1 and 11 and the references claims 1 and 9, Applicants point out the following exemplary differences between Applicants claims 1 and 11 and claims 1 and 9 of the reference:

(1) Applicants claim recites “multiple W-bit data slice latches” and not “a W-bit packet data slice” as in the claims of the reference. Further, there is no teaching in the reference as to handling multiple data slices simultaneously.

(2) Applicants claim recites “a remainder partition comprising multiple XOR subtree levels having remainder latches between remainder XOR subtree levels” not only “a remainder latch” as in the reference. Further “comprising multiple XOR subtree levels having remainder latches between remainder XOR subtree” is not found in the claims of the reference.

(3) Applicants claim “multiple XOR subtree levels” not “a remainder XOR subtree” as in the claims of the reference.

(4) All the limitations of the clause “multiple packet data slice latches each having W-bits where W is a positive integer, each packet data slice latch having inputs and outputs, said packet data slice latches connected in series from a first to a last packet data slice latch, outputs of a previous packet data slice latch connected to inputs of an immediately subsequent packet data slice latch” found in Applicants claims 1 and 11 are not found in the claims of the reference.

(5) All the limitations of the clause “a current cyclic redundancy check (CRC) remainder latch having M-bits where M is a positive integer and having inputs and outputs, the outputs of said combinatorial XOR tree connected to corresponding inputs of said current CRC remainder latch and the outputs of said current CRC remainder latch connected to corresponding inputs of said remainder partition” found in Applicants claims 1 and 11 not found in the claims of the reference.

Applicants contend there are multiple differences between not only the elements of Applicants claims 1 and 11 over the reference claims 1 and 9, but also multiple differences in the connections between elements. Therefore Applicants contend claims 1 and 9 are not unpatentable over claims 1 and 9 of US. 7,103,832 and are in condition for allowance. Since claims 2 through 10 depend from claim 1 and claims 12 through 20 depend from claim 11, Applicants contend claims 2 through 10 and 12 through 20 are likewise in condition for allowance.

Specifically, to Applicants claim 21, Applicants claim 21 includes the following limitations not found in reference claim 17:

“(b) substituting a previous CRC cycle data and corresponding previous CRC remainder for said current CRC remainder or for a previously substituted CRC remainder and adding an additional packet data slice latch, an additional CRC remainder latch, an additional data XOR

tree, an additional remainder XOR tree and an additional combinatorial XOR tree to said CRC circuit design without altering the a CRC remainder result of said CRC circuit design;

(c) partitioning all packet data slice latches and all data XOR trees into a data partition and all additional current CRC remainder latches and all remainder XOR trees into a remainder partition;

(d) combining all remainder XOR trees into a single remainder XOR tree and combining all data XOR trees into a single data XOR tree;

(e) repeating steps (b) through (c) a predetermined number of times; and

(f) distributing said single remainder XOR tree in said remainder partition over two or more remainder XOR subtree levels, distributing all additional CRC remainder latches over one or more remainder latch levels, distributing said single data XOR trees in said data partition over two or more data XOR subtree levels.”

Specifically, to Applicants claim 26, Applicants claim 26 includes the following limitations not found in reference claim 17:

“(a) distributing a current cyclic redundancy check (CRC) remainder XOR calculation of a redundancy check circuit into a remainder partition comprising multiple levels of remainder XOR subtrees and having remainder latches between said levels of remainder XOR subtrees; and

(b) distributing a packet data slice XOR function of said ~~M-bit~~ redundancy check circuit into a data partition of comprising multiple levels of data XOR subtrees and having data latches between said levels of data XOR subtrees.”

Therefore Applicants contend claims 21 and 26 are not unpatentable over claim 17 of US. 7,103,832 and are in condition for allowance. Since claims 22 through 25 depend from claim 21

and claims 27 through 30 depend from claim 26, Applicants contend claims 22 through 25 and 27 through 30 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,

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